A Multilevel Boost Converter Using Switched Inductor

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ABSTRACT

This paper presents a new single stage DC-DC multilevel boost converter topology with very high voltage gain ratio. It is a Pulse width modulation (PWM) based switched inductor multilevel boost converter (SIMLC) consisting of two switched inductors, 2N+2 Diodes, 2N-I Capacitors for N level boost converter. High switching frequency has been used to decrease component size. The proposed converter consists of only one switch. The main advantage of proposed topology is output voltage can be increases by increasing number of capacitors and diodes at output side without disturbing main circuit.

Keywords: Voltage Multiplier, Multilevel Boost Converter, Switched Inductor.

1. INTRODUCTION

The Renewable energy based sources like photovoltaic module, fuel cell give nearly about 15-25V DC output voltage, which is not sufficient for generating 110-220V AC supply voltage for home appliances. To get such high voltage, many PV panels need to be connected in series or another option is to use high voltage gain boost converter. By connecting many PV panels in series, the efficiency of system decreases and also this configuration is sensitive for environmental condition like shading, rainy season. So the best option to get high voltage is use high gain boost converter. There are different DC-DC boost converters [2] with high voltage gain ratio as given in table 1.

The gain ratio of simple boost converter is low, also voltage stress across switch is same as output voltage. For switched inductor boost converter gain ratio increases but voltage stress across switch is same as output voltage. The advantage of multilevel boost converter is gain increases but stress is less as compared to other converter topology [3]. In switched inductor multilevel converter gain ratio is high compared to multilevel converter and stress is also lower than multilevel boost converter for same duty cycle [1].

The efficiency of proposed switched inductor multilevel boost converter (SIMLBC) is high because of only one switch is used. The diode D1-D5 and capacitor C1-C5 form voltage multiplier stages [4]. The main advantage of proposed topology is output voltage can be increase by increasing number of capacitors and diodes means multiplier stages without disturbing main circuit.

Table 1 Different Boost Topology with Gain Ratio

<table>
<thead>
<tr>
<th>No.</th>
<th>Type</th>
<th>Voltage Gain Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Simple Boost Converter</td>
<td>$\frac{1}{1 - D}$</td>
</tr>
<tr>
<td>2</td>
<td>Multilevel Boost Converter</td>
<td>$\frac{N}{1 - D}$</td>
</tr>
<tr>
<td>3</td>
<td>Switched Inductor Boost Converter</td>
<td>$\frac{(1 + D)}{(1 - D)}$</td>
</tr>
<tr>
<td>4</td>
<td>Switched Inductor Multilevel Boost Converter</td>
<td>$\frac{N(1 + D)}{(1 - D)}$</td>
</tr>
</tbody>
</table>
2. OPERATION MODES

The proposed topology consist of two switched inductors, 2N+2 Diodes, 2N-1 Capacitors and single switch for N level DC-DC boost converter. Schematic diagram of proposed converter for three levels is as shown in fig1.

The operation of proposed topology is similar to conventional boost converter. The inductor L₁ and L₂ are charges in parallel when switch S₁ is ON and discharge in series when switch S₁ is in OFF mode. The operation of circuit divided in two modes [1],[2],[3].

2.1 Mode 1 (Switch S₁ closed)

When the switch S₁ closes, both switched inductor charges through diodeDS₁ and DS₃ as shown in fig.2. In this mode DS₂ diode is not working. On the same time at output side if capacitor C₁ has higher voltage than Capacitor C₄ then capacitor C₁ charges Capacitor C₄ through diode D₂. As capacitor C₄ get fully charged it reverse bias diode D₂. As soon as diodes D₂ reverse bias capacitor C₁ and C₂ charges capacitor C₄ and C₂ through D₄ diode.

This operation continues up to N level and this happen in very short period of time.
2.2 Mode 2 (Switch $S_1$ open)

As switch $S_1$ is open, the energy stored in switched inductor $L_1$ and $L_2$, and Capacitor $C_4$ and $C_5$ has given to output side capacitor to give higher output voltage.

The combine voltage of input source and both switched inductor is initially given to capacitor $C_1$ through diode $D_1$. As capacitor $C_1$ is fully charged it reverse bias diode $D_1$ then capacitor $C_2$ gets charge through diode $D_3$. Similarly when capacitor $C_2$ is fully charged it reverse bias diode $D_3$. Then capacitor $C_3$ is charge through diode $D_5$. So total voltage across capacitors $C_1+C_2+C_3$ is a summation of voltage of input source, voltage across inductor $L_1$, $L_2$ and two capacitor $C_4$, $C_5$.

Mode of operation shown in fig.3.

3. **ANALYSIS OF PROPOSED TOPOLOGY**

Fig.4 shows conventional boost converter, when switch $S_1$ is ON for $DT_s$ the inductor gets charged. As Switch $S_1$ gets OFF, the stored energy of inductor is transferred to load along with input energy. Assuming current through inductor and voltage across capacitor is constant, at steady state condition voltage across inductor is ideally [3]-[6]

$$V_L = D V_{in} - (1 - D)(V_{in} - V_o) = 0 \quad (1)$$

Where D is duty cycle, $V_{in}$ is input voltage.
\( V_O \) is output voltage

From equation (1) it gives output voltage as

\[
\frac{V_O}{V_{in}} = \frac{1}{(1-D)} \tag{2}
\]

As current through inductor is given by equating input power and output power by neglecting losses,

\[
V_{in} I_L = V_O I_O = \frac{V_O^2}{R_c} \tag{3}
\]

\[
I_L = \frac{V_O}{V_{in}R_O} = \frac{V_O}{(1-D)R_O} \tag{4}
\]

Now consider switched inductor multilevel converter consisting of two inductors and \( N \) capacitors as shown in fig.1. When switch \( S_1 \) is closed the two inductors are in parallel so voltage across them is same but current is divided, and when switch \( S_1 \) is in OFF condition both the inductors are in series so current is same but voltage is divided. As switch \( S_1 \) is closed input energy is initially stored in parallel inductors, as switch \( S_1 \) is OFF the stored energy is transferred to load. As in steady state condition and losses are neglected, the voltage across inductor is \([1,6]\)

\[
V_L = D V_{in} - (1-D) \left( \frac{V_{in}}{2} - \frac{V_O}{N} \right) = 0 \tag{5}
\]

Eq. (5) gives output voltage as

\[
\frac{V_O}{V_{in}} = \frac{N(1+D)}{(1-D)} \tag{6}
\]

Current through inductor is

\[
I_L = \frac{N V_O}{(1-D)R_O} \tag{7}
\]

Where \( N \) is no. of level

Now considering power loss in inductor which limits the theoretical value of boosting factor, \( R_L \) is internal resistance of inductor then eq.(5) becomes \([1]\)

\[
V_L = D V_{in} - (1-D) \left( \frac{V_{in}}{2} - \frac{V_O}{N} - I_L R_L \right) = 0 \tag{8}
\]

\[
V_{in} (1+D) = i_L R_L + \frac{V_O}{N} (1-D) \tag{9}
\]

By eq. (7) and (9)

\[
V_{in} (1+D) = \frac{NV_o R_L}{(1-D)R_O} + \frac{V_O}{N} (1-D) \tag{10}
\]

\[
\frac{V_O}{V_{in}} = \frac{1}{(1-D) \frac{R_L N}{N(1+D)(1-D)R_O}} \tag{11}
\]
The inductor and capacitor size is chosen such that change in current through inductor is not more than 5% of average current of inductor and ripple voltage across capacitor is less than 5% of average capacitor voltage [2].

\[
L = \frac{D(1-D)^2 R}{2N^2} \quad (12)
\]

\[
C = \frac{D\Delta V_{\text{out}}}{FR\Delta V_c} \quad (13)
\]

Where \( \Delta V_c \) is change in capacitor voltage

\[ F \] is switching frequency

\[ R \] is load resistance

4. SIMULATION RESULT

The simulation was carried out in PSpice software for no. of level is 3, the parameter values were chosen according to derived formulae of inductor and capacitor. The electronic switch IRF540 and diode MUR460 used for simulation. 50 KHz switching frequency had been chosen to reduce component size. The parameter value is listed in table no.2.

The output voltage is taken across load and it is summation of output capacitors \( C_1+C_2+C_3 \). The output voltage is 148.36V for input 15V which give voltage gain ratio 9.89 as shown in fig.5. The voltage across output capacitor \( C_1,C_2,C_3 \) are nearly same and equal to 50V shown in fig.6. The voltage stress across switch was 53.6V for 60% duty cycle which was very low as compared to conventional boost converter or other topology, and it is 36.12\% of output voltage shown in fig.7. The voltage stress across diode \( D_1 \) to \( D_5 \) are same and equal to 50.2V which is 33.83\% of output voltage show in fig.8.

<table>
<thead>
<tr>
<th>No.</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input Voltage</td>
<td>15V</td>
</tr>
<tr>
<td>2</td>
<td>Output Voltage</td>
<td>148.36V</td>
</tr>
<tr>
<td>3</td>
<td>Inductor ( (L_1,L_2) )</td>
<td>10mH</td>
</tr>
<tr>
<td>4</td>
<td>Capacitor (all are same value)</td>
<td>100( \mu )F</td>
</tr>
<tr>
<td>5</td>
<td>Switching Frequency</td>
<td>50 KHz</td>
</tr>
<tr>
<td>6</td>
<td>Output Power</td>
<td>220.10W</td>
</tr>
<tr>
<td>7</td>
<td>Load Resistance</td>
<td>100( \Omega )</td>
</tr>
<tr>
<td>8</td>
<td>Duty Cycle</td>
<td>60%</td>
</tr>
</tbody>
</table>

Table 2 Parameter Value

Fig.5. Output Waveform
Fig. 6 Voltage Stress Across Switch

Fig. 7 Voltage Stress Across Switch

Fig. 8 Voltage across diode D₁ to D₅ are same
5. CONCLUSION

In this paper multilevel dc-dc boost converter is presented for obtain higher voltage gain 9.87 for three levels which is very high compared to conventional dc-dc converter and multilevel topology. The voltage stress across switch and output diodes are very less as compared to output voltage which increases efficiency of proposed topology. The mathematical analysis and circuit operation discussed. The simulation result provided in the paper validated the proposed topology. The advantage of proposed topology is output voltage can be increases by increasing number of capacitors and diodes without disturbing main circuit.

REFERENCES


