FPGA Based 70MHz Digital Receiver for RADAR Applications

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ABSTRACT

At present there has been a great demand for wireless communications technology. The digital receiver must be communicated with all the new wireless standards. This receiver is used for obtaining the information from the target devices, in RADARs. After receiving the information, the parameters like speed, distance and angle of the target device are calculated. In this paper proposed a 70MHz digital receiver which has high sampling rate for narrow band or wide band digital signals. In digital receiver there is digital down converter (DDC) which is used for frequency translation and better decimation factor. After implementation, got higher precision and more stability of the signal compared to analog counterparts. The entire architecture of digital receiver captured on FPGA device using ADC daughter card.

Keywords: Digital Receiver, RADAR, Digital down converter, FPGA and ADC.

I. INTRODUCTION

In recent years, there has been a great demand for wireless communications technology. As a result of this increasing demand, several new wireless communication standards have been created and put into use. With the advent of all of these different wireless standards, it is desirable to have a radio receiver that is capable of communicating with several different standards. The digital receivers are now-a-days being widely used and replacing the analog receivers as they are capable of achieving much higher precision and stability than their analog counterparts.

[1] Narrow band digital receiver finds applications in communication signal processing. This digital receiver having required band width is going to be used for linear frequency modulation radar signal processing. [1], [2] Sampling frequency used here is 160 Msps. Different applications require different bandwidths. According to bandwidth, design parameters should be changed.

Wireless [3], [7] RF receivers are used in a range of applications, including wireless security systems, industrial monitoring, meter reading, and home automation. In the past, semiconductor suppliers primarily built these receivers using analogue designs. Today, suppliers are transitioning to digital and mixed-signal designs to reduce power consumption and ease of integration with other components. In the case of a global system for mobile communications (GSM) system, the frequency of the incoming signal at this stage is around 70 MHz. This high-frequency signal then passes through a digital down converter (DDC), which performs frequency translation and produces the corresponding baseband signal. [7] In the case of a GSM system, the baseband frequency is around 270 KHz.
The GSM pass band bandwidth of interest is 80 KHz. The GSM requirements for the overall response of the three-stage multi-rate filter of the DDC includes, decimating the input signal by 256; less than 0.1 dB of peak-to-peak pass-band ripple; and 18 dB of attenuation at 100 KHz [3].

This design concentrates [6] on the three-stage multi-rate decimation filter, which includes a compensated integrated comb (CIC) filter and two decimating finite impulse response (FIR) filters. The CIC filter is suitable for this high-speed application (69.333 MHz) because of its ability to achieve high decimation factors and the fact that it's implemented without using multipliers. The CIC in this example will perform decimation by 64. [16] The second filter is a 21-tap CIC-compensation FIR (CFIR) filter, which has an inverse-sync pass-band response, and decimates by two. [2] The third-stage filter is a 63-tap programmable FIR (PFIR) filter, which ensures that the overall filter response meets the GSM spectral mask. It also decimates by two to achieve an overall decimation factor of 256. Intermediate frequency is decided by the RF design engineers.

ADC daughter card has a four channel ADC/DAC daughter card. This provides two 14-bit A/D channels and two 16-bit D/A channels which can be clocked by an internal clock source or an externally supplied sample clock. It has a low-pin count connector and a front panel I/O. The ADC daughter card complies with the FMC standard. It is a single width conduction cooled mezzanine module in which the front area holds 6 MMCX or SSMC connectors available from the front panel [13].

Here, the intermediate frequency signal of 70 MHz is applied as input to the ADC daughter card [13]. The ADC converts analog signal into digital signal at higher sampling rate more than 160Msps. This signal will be given as input to the digital down converter.

II. PROPOSED DIGITAL RECEIVER

Figure 1 shows the block diagram of digital receiver implemented in FPGA. Function generators are used to generate IF signal and clock signal. After digitizing the input IF signal the output will be in double data rate. This double data rate is converted to single data rate using IP primitives in UNISIM library. Now, the ADC is interfaced to the FPGA by writing HDL code.

![Digital Receiver implemented in FPGA](image)

Figure 1: Digital Receiver implemented in FPGA

Now, the digitized signal is given as input to the digital down converter (DDC) which is used for frequency translation and decimation factor. This DDC is implemented by using IP cores. The advantage of DDC is we can change the code as per the user requirement.
In DDC, mainly there are four blocks which are of IP cores like direct digital synthesis (DDS), CIC filter, CFIR filter and PFIR filter. At each stage of filtering sections, the signal is filtered and decimated to get final base band signal.

The Micro Blaze is a virtual microprocessor that is built by combining blocks of code called cores inside a Xilinx Field Programmable Gate Array (FPGA). The beauty to this approach is that it will only end up with as much microprocessor as required. The Micro Blaze processor is a 32-bit Harvard Reduced Instruction Set Computer (RISC) architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory at the same time. The backbone of the architecture is a single-issue, 3-stage pipeline with 32 general-purpose registers, an Arithmetic Logic Unit (ALU), a shift unit, and two levels of interrupt. This basic design can then be configured with more advanced features to tailor to the exact needs of the target embedded application such as: barrel shifter, divider, multiplier, single precision floating-point unit (FPU), instruction and data caches, exception handling, debug logic, Fast Simplex Link (FSL) interfaces and others. This flexibility allows the user to balance the required performance of the target application against the logic area cost of the soft processor.

Micro Blaze [15] is a soft-core microprocessor, any optional features not used will not be implemented and will not take up any of the FPGAs resources. The Micro Blaze pipeline is a parallel pipeline, divided into three stages: Fetch, Decode, and Execute. In general, each stage takes one clock cycle to complete. Consequently, it takes three clock cycles (ignoring delays or stalls) for the instruction to complete. Each stage is active on each clock cycle so three instructions can be executed simultaneously, one at each of the three pipeline stages. Micro Blaze implements an Instruction Pre-fetch Buffer that reduces the impact of multi-cycle instruction memory latency. While the pipeline is stalled by a multi-cycle instruction in the execution stage the Instruction Pre-fetch Buffer continues to load sequential instructions. Once the pipeline resumes execution the fetch stage can load new instructions directly from the Instruction Pre-fetch Buffer rather than having to wait for the instruction memory access to complete. The Instruction Pre-fetch Buffer is part of the backbone of the Micro Blaze architecture and is not the same thing as the optional instruction cache.

III. RESULTS

Design code is verified using test bench. The results shown in figure 2 are observed using ISE software.

Two ADC signals of double data rate are converted to single data rate using IP primitives. Got double data rate of 14 bit digital data. This signal is filtered through three filter sections. Finally got required digital data.
Results shown from figures 3 to 8 are observed in MATLAB. The signal frequency components can be checked by using fast fourier transform (FFT) technique. Individual part of the design is verified with FFT. Response of the different filters is verified with different input signals.

The generated input signal which is to be applied to the multiplier is shown in figure 3.

![Figure 3: Input Signal](image)

Input signal generated using MATLAB and is applied to multiplier. Using FFT technique, frequency of 71.5 MHz is generated which is a required one.

DDS output shown in figure 4.

![Figure 4: DDS Output](image)

Generated output frequency of 70MHz from the numerically controlled oscillator or DDS.

Multiplier output shown in figure 5.

![Figure 5: Multiplier output](image)

Output is having 1.5 and 141.5 MHz components. This signal is filtered.

CIC filter output shown in figure 6. After getting baseband signal there is some droop in the CIC output filter.
CFIR filter output shown in Figure 7. Here the droop that occurred in CIC filter will be solved by using compensation FIR technique.

![Figure 7: CFIR output](image)

Finally we have 1.5 MHz signal at the output, which is the expected output. Results shown in figure 9 to 13 are observed in CRO.

The input IF signal is generated using function generator as shown in figure 9.

![Figure 9: Output of ADC](image)

The input signal is beaten with the 70 MHz frequency which is generated by using direct digital synthesis (DDS) as shown in figure 10.

![Figure 10: Output of DDS](image)

PFIR output shown in figure 8. For any modification in the filter that we want to change will be configured by using programmable FIR technique.

![Figure 8: PFIR output](image)
The input IF signal and DDS signal are given as input to the mixer. As shown in figure 11 both signals are mixed to get the base band signal.

Figure 11. Output of Mixer

The base band signal is filtered using CIC filter and got some droop in the signal as shown in figure 12.

Figure 12: output of CIC filter.

The droop obtained in CIC filter section is eliminated using CFIR filter section which is shown in figure 13.

Figure 13: Output of CFIR filter.

IV. CONCLUSION

In this paper, designed and implemented a narrow band digital receiver with intermediate carrier frequency of 70 MHz using Xilinx IP cores. After filtering and decimation through different filtering sections in DDC, got baseband signal. Finally, got required baseband signal with minimum noise and more spectral purity.
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