Implementation of Mod-16 Counter using Verilog-A Model of CNTFET

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ABSTRACT

Carbon Nanotube Field Effect Transistor (CNTFET) has a wide scope in the field of Nanotechnology. These are currently considered as the replacement to the Si MOSFET. These devices show the ballistic transport in the current conduction. In this paper, a Verilog-A formulation of the Stanford compact model is used for the simulation of different logic gates in Cadence and finally Mod-16 Counter is simulated. The outputs of the simulations have been extensively studied. When then outputs of CNTFET are compared with that of silicon technology, CNTFET shows much better device performance in terms of power.

Keywords: CNTFET, Cadence, Logic Gates, Mod-16 Counter.

1. INTRODUCTION

For many decades, MOSFETs are being used as a basic building block for most of the electronic devices [1]. But we know that the number of transistors on integrated circuits doubles approximately every two years as per Moore’s law. Therefore, to keep pace with this trend of smaller device size, high device density, less power dissipation and high device speed CNTFET is considered as an alternate choice of MOSFET [2].

In recent years, many efforts have been made in the modeling and simulation of molecular devices. And the results indicate that the current VLSI fabrication techniques like lithographic patterning can hardly be extended to a few nm in gate channel region. Even if such device can be fabricated, the cost for sophisticated lithography and patterning techniques keep skyrocketing thereby leading to the end of Moore’s law. Hence there should be a radical paradigm shift from existing silicon technology to the molecular devices. Hence CNTFETs are being explored to prolong Moore’s law. Several such nano devices are currently being researched, such as resonant tunneling diode (RTD), the single-electron transistor (SET) and spin transistor (SPINFET) [4]. In general, nano-science research focuses primarily on the search for new physical concepts and on creating the technology necessary for the development of nano devices. But the physical characteristics of CNTFETs, as well as their versatility and maturity, put CNTFETs among the most promising molecular devices[5].

In this paper, a Verilog-A formulation of the Stanford compact model has been used for the simulation of different logic gates in Cadence. Initially, a brief introduction about the Carbon nano tube electronics is given, followed by the detailed explanation of structure and modeling aspects of CNTFET. Finally, the simulation results of various CNTFET logic circuits such as NOT gate, two input NAND gate, three input NAND gate, JK flip flop and Mod-16 Counter have been discussed.
2. CARBON NANOTUBE ELECTRONICS

Carbon Nano Tubes are nothing but hollow cylinders in which one or more concentric layers of carbon atoms in a honey comb lattice arrangement are present [6]. Carbon nanotubes exist as a macro-molecule of carbon, analogous to a sheet of graphite rolled into a cylinder. SWCNT (Single Walled Carbon Nano Tube) and MWCNT (Multi Walled Carbon Nano Tube) are the two types of CNT[7]-[9]. SWCNT can further be classified into Arm-Chair, Zigzag and Chiral which can be described by the chiral vector (n, m), where n and m are the integers of the vector equation \( R = n\mathbf{a}_1 + m\mathbf{a}_2 \).

![Fig. 1. Three Types Of Carbon Nano Tube](image1)

![Fig. 2. Representation of Chiral Vector](image2)

The values of n and m determine the chirality, or "twist" of the nanotube. The chirality in turn affects the diameter and hence the conductance of the carbon nanotube. A SWNT is considered metallic if the value \( n - m \) is divisible by three, otherwise the nanotube is semiconducting.

3. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

CNTFET is basically MOSFET like structure which has semiconducting carbon nanotube as conducting channel. It can also be defined as a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. [10]

![Fig. 3. Carbon Nanotube Field Effect Transistor](image3)
We have already discussed that CNT can be single walled or multi walled depending on the number of concentric nanotube cylinders. The length of the nanotube acts as the channel of a transistor between metal source and drain. The width of the nanotube cannot be changed to increase the current drive because once a nanotube is grown, it has fixed diameter. But we can increase the current drive of CNTFET by adding more nanotubes in parallel. A carbon nanotube’s band-gap is directly affected by its chirality and diameter. The diameter and different Vth of the CNT can be calculated based on the following equations [11]-[13]

\[ V_{th} \approx \frac{E_g}{2e} = \frac{aV_{\pi}}{\sqrt{3}D_{CNT}} \]  
\[ D_{CNT} = \frac{\sqrt{3}a_o\sqrt{n^2+m^2+nm}}{\pi} \]

where \( a_o = 0.142 \) is the interatomic distance between each carbon atom and its neighbour.

4. DESIGN DETAILS AND SIMULATION RESULTS

In this section, logic circuits and simulations are discussed one by one. Those logic circuits which are used to simulate the Mod-16 Counter are presented first.

4.1 NOT Gate

In fig. 4 and 5, the schematic diagram and the simulation output of a NOT gate using CNTFET are shown respectively. In fig. 5, we can easily observe that the output provides LOW and HIGH values when the input is HIGH and LOW respectively.

Fig. 4. Not Gate Using CNTFET

Fig. 5. Simulation Output of Not Gate
4.2 Two-Input NAND Gate

Fig. 6 and fig. 7 represent the schematic diagram and simulation output of a 2-input NAND gate. From the simulated output waveform we can observe that if either inputs or any one of the input is LOW then the output is high otherwise the output is LOW.

Fig. 6. two-input nand gate using CNTFET

4.3 Three Input NAND Gate

The schematic and the simulation output of a 3-input NAND gate is shown in fig. 8 and fig. 9 respectively. If all the three inputs or any one of the input is LOW then the output is HIGH if all the three inputs are HIGH, then the output will be LOW as shown in fig. 9.

Fig. 8. Three-Input Nand Gate Using CNFTFET
4.4 JK Flip-Flop

JK flip flop is the most versatile of the basic flip flops. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states [1]. It can also perform toggling action as a T flip-flop if J and K are tied together. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high, at the clock edge then the output will toggle from one state to the other as shown in fig. 11. Here, the schematic of JK flip-flop is made with the help of cell structure of the gates created from the schematic of the respective gates as shown in fig. 10.

![Fig. 10 jk flip-flop using cntfet](image)

![Fig. 11 Simulated Output of JK Flip-Flop Using CNTFET](image)
4.5 Mod-16 Counter

A counter is a sequential digital circuit whose output progresses in a predictable repeating pattern with each beat of the clock. In mod-16 counter 4 JK flip-flops are used in their toggling mode (J and K both are HIGH). In this type of counter the output of one flip-flop acts as a clock for the next flip-flop.

Fig. 12. Mod-16 Counter Using Cntfet

Fig. 13. Simulated Output Of Mod-16 Counter

5. CONCLUSION

Carbon Nanotube Field Effect Transistor provides a vast field of research in the area of nanoelectronics. A number of different logic designs can be implemented using CNTFET concept which will be very useful in designing of different digital and mixed signal circuits. In this work, Mod-16 Counter along with other logic designs is simulated in Cadence using the Verilog-A model of CNTFET. These logic circuits using CNTFET, promises a better alternative for MOSFETS.
REFERENCES


